EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6	over$1clock$3 near2 detect$3	USPAT	OR	OFF	2006/02/15 11:18
S2	4	over$1clock$3 near2 detect$3	US-PGPUB	OR	OFF	2006/02/15 11:40
S3	0	over$1clock$3 near2 detect$3	EPO; JPO; IBM_TDB	OR	OFF	2006/02/15 11:44
S4	13	("6535988").URPN.	USPAT	OR	OFF	2006/02/15 13:23
S5	6	("5592111" | "5671195" | "5696950" | "5713030" | "6055645" | "6211744").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/02/15 13:25
S6	10	("5592111").URPN.	USPAT	OR	OFF	2006/02/15 13:54
S7	20	("3764992" | "3831113" | "3852616" | "3906247" | "3990007" | "4063308" | "4263565" | "4359649" | "4380746" | "4447870" | "4564837" | "4615005" | "5086387" | "5089955" | "5101127" | "5107523" | "5180935" | "5274337" | "5280605" | "5440254").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/02/15 14:10
S8	6	("5734274").URPN.	USPAT	OR	OFF	2006/02/15 14:14
S9	6	("5151611" | "5410186" | "5410196" | "5485105" | "5508638" | "5592111").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/02/15 14:29
S10	6	("6385735").URPN.	USPAT	OR	OFF	2006/02/15 15:11
S11	1697	feedback near2 clock	USPAT	OR	OFF	2006/02/15 15:55
S12	43	feedback near2 clock with processor	USPAT	OR	OFF	2006/02/15 15:55
S13	1	feedback near2 (clock adj (rate frequency)) with processor	USPAT	OR	OFF	2006/02/15 15:56
S14	71	feedback near2 (clock adj (rate frequency))	USPAT	OR	OFF	2006/02/15 15:58
S15	0	feedback near2 (clock adj (rate frequency)) and (over$1clock$3 (speed adj governor) (clock adj limit$3))	USPAT	OR	OFF	2006/02/15 15:57
S16	1	feedback near2 (clock adj (rate frequency)) near10 (processor cpu)	USPAT	OR	OFF	2006/02/15 15:58
S17	1	feedback near2 (clock adj (rate frequency)) same (processor cpu)	USPAT	OR	OFF	2006/02/15 15:58
S18	2001	speed adj governor	USPAT	OR	OFF	2006/02/15 16:07
S19	33	speed adj governor and (clock with (processor cpu))	USPAT	OR	OFF	2006/02/15 16:07
S20	0	tri$1state near3 processor with memory with reset	USPAT	OR	OFF	2006/02/16 10:59

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S21	13	tri$1state near3 processor with reset	USPAT	OR	OFF	2006/02/16 11:28
S22	23	tri$1state near3 processor with memory	USPAT	OR	OFF	2006/02/16 11:01
S23	0	tri$1state near3 processor and (over$1clock$3 speed$1govern$3 speed$1limit$4)	USPAT	OR	OFF	2006/02/16 11:06
S24	0	(tri$1state adj unit) near3 processor	USPAT	OR	OFF	2006/02/16 11:06
S25	0	(tri$1state adj unit) with (processor cpu)	USPAT	OR	OFF	2006/02/16 11:06
S26	3	tri$1state near3 cpu with reset	USPAT	OR	OFF	2006/02/16 11:27
S27	1	tri$1state near3 processor with reset	EPO; JPO; IBM_TDB	OR	OFF	2006/02/16 11:30
S28	2	tri$1state near3 processor with reset	US-PGPUB	OR	OFF	2006/02/16 11:30
S29	46	tri$1state with reset with (processor cpu)	USPAT	OR	OFF	2006/02/16 11:42
S30	14	tri$1state adj unit	USPAT	OR	OFF	2006/02/16 11:57
S31	242	tri$1state adj circuit	USPAT	OR	OFF	2006/02/16 11:57
S32	4	(tri$1state adj circuit) near5 (processor cpu)	USPAT	OR	OFF	2006/02/16 11:57
S33	111	"AND" near2 tri$1state	USPAT	OR	OFF	2006/02/16 12:58
S34	3	("AND" near2 tri$1state) with reset	USPAT	OR	OFF	2006/02/16 13:04
S35	1	("AND" near2 tri$1state) with reset	US-PGPUB	OR	OFF	2006/02/16 13:04
S36	0	("AND" near2 tri$1state) with reset	EPO; JPO; IBM_TDB	OR	OFF	2006/02/16 13:04
S37	3033	enabl$3 near5 tri$1state	USPAT	OR	OFF	2006/02/16 13:08
S38	267	enabl$3 near5 tri$1state with "AND"	USPAT	OR	OFF	2006/02/16 13:08
S39	140	enabl$3 near5 tri$1state with "AND" with signal	USPAT	OR	OFF	2006/02/16 13:08
S40	82	enabl$3 near5 tri$1state with "AND" with enable adj signal	USPAT	OR	OFF	2006/02/16 13:09
S41	3	enabl$3 near5 tri$1state with "AND" with enable adj signal same processor	USPAT	OR	OFF	2006/02/16 13:09